EE221 – Logic Systems Design I

Problem Set 6
Due October 28, 2009

1. What is the minimum number of bits required to represent -143_{10} as a signed binary number in 2’s complement form?

2. What is the decimal value of the 2’s complement signed binary number 100000000?

3. Express -12_{10} as a 5-bit, 2’s complement signed binary number.

4. Using your result from the previous problem as a starting point, show the steps to express +12_{10} as a 5-bit signed binary number.

5. What is the decimal value of the 2’s complement signed binary number 110101101?

6. Perform the following binary subtraction using 2’s complement addition: 43 – 47 = ____. Express your answer as a decimal integer (show your steps in determining the decimal value from the binary sum).

7. Perform the following binary subtraction using 1’s complement addition: 37 – 23 = ____.

8. Perform the following binary subtraction using 2’s complement addition: 37 – 23 = ____.

9. Perform the following binary addition using 2’s complement arithmetic: -67 – 28 = _____. Express your answer as a decimal integer (show your steps in determining the decimal value from the binary difference).

10. Perform the following 2’s complement addition: 100001 + 100010 = ____. State whether or not an overflow occurs. Justify your answer.
11. Write a VHDL entity and architecture for a 4-to-1 multiplexer. Use the WITH-SELECT construct. State how you would verify this design in simulation. Simulate your design.

12. Starting with the design you created in the previous problem, write a VHDL entity and architecture for a multiplexer which takes in four 4-bit channels and outputs a single 4-bit channel. Simulate your design.

13. Write a VHDL entity and architecture for an 4-to-2 priority encoder. Use a PROCESS statement and the IF-THEN construct. State how you would verify your design in simulation. Simulate your design.