cadence

2

Creating a schematic design

This chapter consists of the following sections:

Objective

To create a schematic design in OrCAD Capture. In this chapter, you will be introduced to basic design steps, such as placing a part, connecting parts using wires, adding ports, generating parts, and so on.

The steps for preparing your design for simulation using PSpice and for taking your design for placement and routing to OrCAD Layout or OrCAD PCB Editor are also covered in this chapter.

Design example

In this chapter, you will create a full adder design in OrCAD Capture. The full adder design covered in this tutorial is a complex hierarchical design that has two hierarchical blocks referring

to the same half adder design.

Duration:

40 minutes

Creating a design in Capture

Guidelines

When creating a new circuit design in OrCAD Capture, it is recommended that you follow the guidelines listed below.

Avoid spaces in pathnames and filenames. This is necessary to get your design into downstream products, such as SPECCTRA for OrCAD.

Avoid using special characters for naming nets, nodes, projects, or libraries. While naming nets, use of illegal characters listed below might cause the netlister to fail.

? (question mark)

@ (at symbol)

~ (telda)

#(hash)

& (ampersand)

% (percent sign)

" (quotation marks)

! (exclamation mark)

( )(parenthesis)

< (smaller than)

= (equal)

> (greater than)

[ ](square parenthesis),

* (asterisk)

Creating a project

To create a new project, we will use Capture's Project Wizard. The Project Wizard provides you with the framework for creating any kind of project.

Launch Capture.

From the File menu, choose *New > Project*.

In the New Project dialog box, specify the project name as `FullAdd`.

To specify the project type, select *Analog or Mixed A/D*.

Note: An Analog or Mixed A/D project can easily be simulated using PSpice. It also ensures that your design flows smoothly into OrCAD Layout for your board design.

Specify the location where you want the project files to be created and click OK.

In the Create PSpice Project dialog box, select the *Create a blank project* option button.

Note: When you create a blank project, the project can be simulated in PSpice, but libraries are not configured by default. When you base your project on an existing project, the new project has same configured libraries.

Click OK to create the FullAdd project with the above specifications.

Tip   In case you already have a schematic design file (`.dsn`) that you want to simulate using PSpice, you need to create an Analog or Mixed A/D project using the *File > New > Project* command and then add your design to it.

The FullAdd project is created. In the Project Manager window, a design file, `fulladd.dsn`, is created. Below the design file, a schematic folder with the name `SCHEMATIC1` is created. This folder has a schematic page named `PAGE1`.

Renaming the schematic folder and the schematic page

You will now modify the design to change the name of both the schematic folder and the schematic page, to HALFADD.

In the Project Manager window, right-click on SCHEMATIC1.

From the pop-up menu, select *Rename*.

In the Rename Schematic dialog box, specify the name as `HALFADD`.

Similarly, right-click on PAGE1 and from the pop-up menu select *Rename*.

In the Rename Page dialog box, specify the page name as `HALFADD` and click OK.

After renaming of the schematic folder and the schematic page, the directory structure in the Project Manager window should be to similar to the figure below.
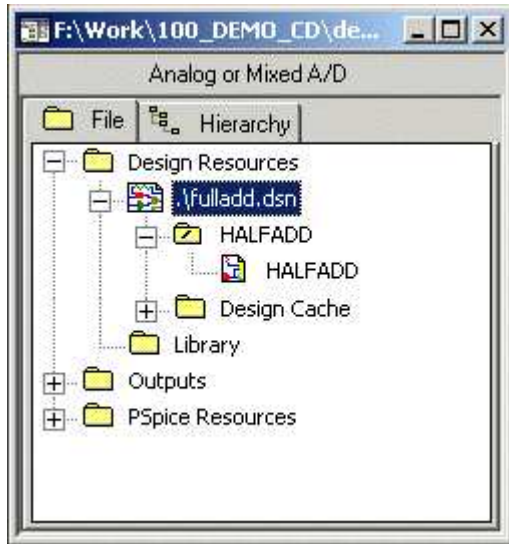
Using a design template

Before you start with the design creation process in OrCAD Capture, you can specify the default characteristics of your project using the design template. A design template can be used to specify default fonts, page size, title block, grid references and so on. To set up a design template in OrCAD Capture, use the Design Template dialog box.

→   - To open the Design Template dialog box, from the Options drop-down menu choose Design Template.

To know more about setting up the design template, see *OrCAD Capture User's Guide*.

Creating a flat design

In this section, we will create a simple flat half adder design with X and Y as inputs and SUM and CARRY as outputs.
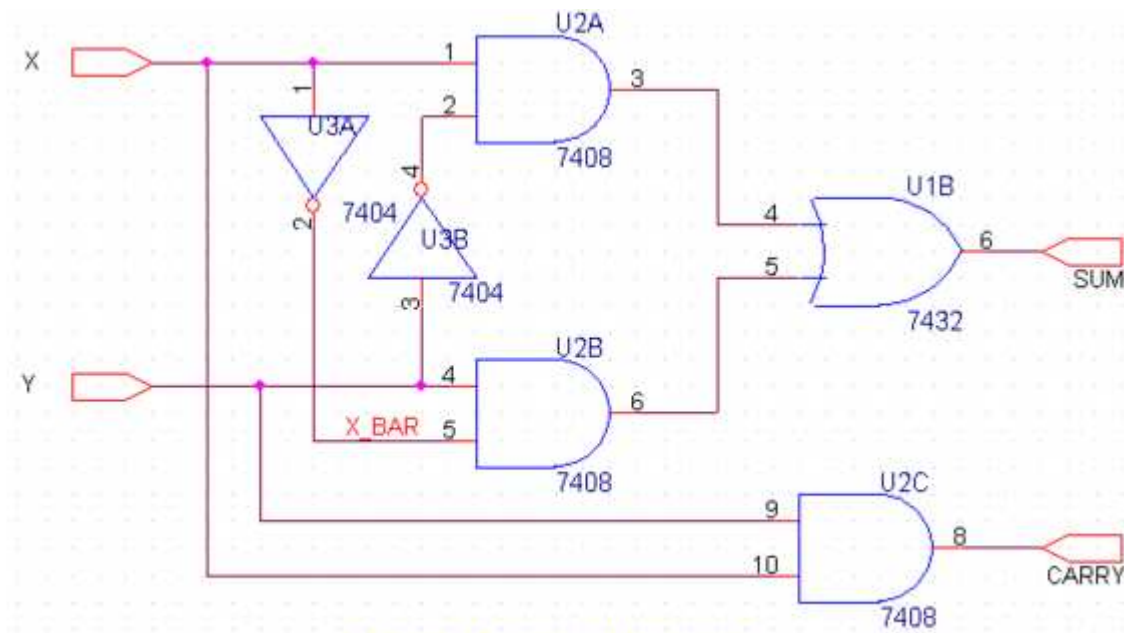
Figure 2-1 Half adder design

Adding parts

To add parts to your design:

From the Place menu in Capture, select Part.

In the Place Part dialog box, first select the library from which the part is to be added and then instantiate the part on the schematic page.

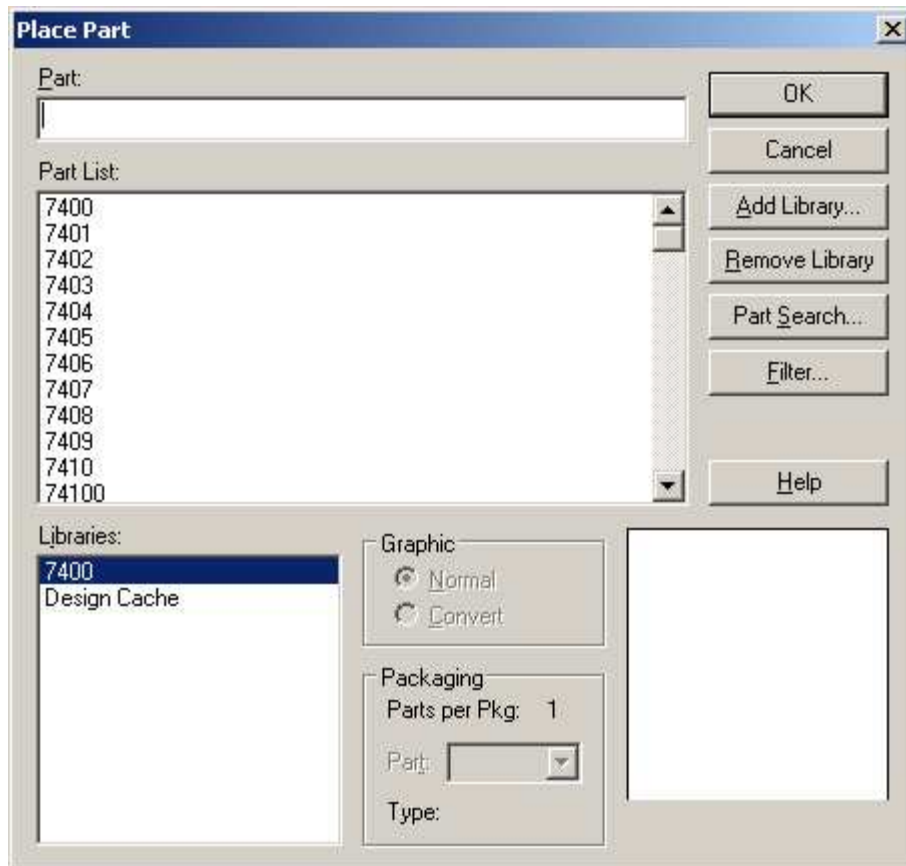The gates shown in Figure 2-1 are available in the `7400.OLB`.

Tip   Use the Part Search button in the Place Part dialog box, to search the library to which the required part belongs.

To add `7400.OLB` to the project, select the Add Library button.

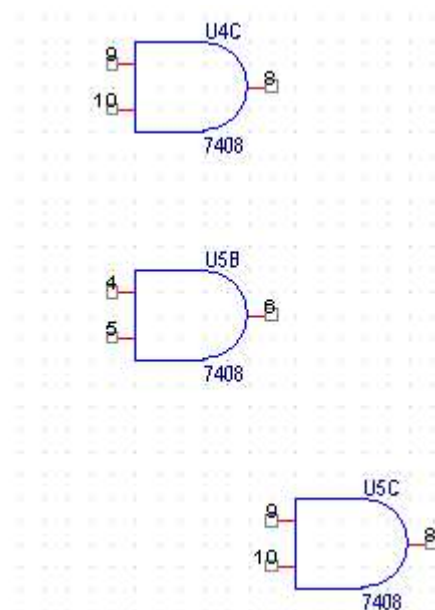Browse to *<install_dir>/tools/capture/library/pspice/7400.olb*.

Select `7400.OLB` and click Open.

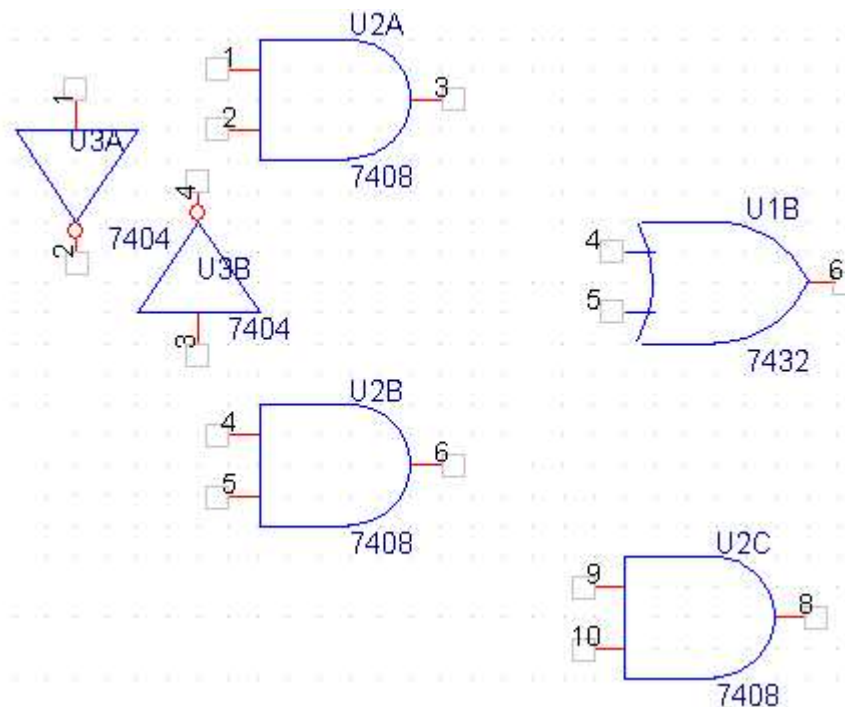The 7400 library appears in the *Libraries* list box.

From the Part List, select 7408 and click OK.

Place three instances of the AND gate, 7408, on the schematic page as shown in the figure below.

Right-click and select *End Mode*.

Similarly, place an OR gate (7432) and two NOT gates (7404) as shown in the figure below.

Connecting parts

After placing the required parts on the schematic page, you need to connect the parts.

From the Place menu, choose Wire.

The pointer changes to a crosshair.

Draw the wire from the output of the AND gate, U2A, to the one of the inputs of the OR gate, U1B. To start drawing the wire, click the connection point of the output pin, `pin3`, on the AND gate.

Drag the cursor to input pin, `pin4`, of the OR gate (7432) and click on the pin to end the wire.

Clicking on any valid connection point ends a wire.

Similarly, add wires to the design until all parts are connected as shown in the figure below.
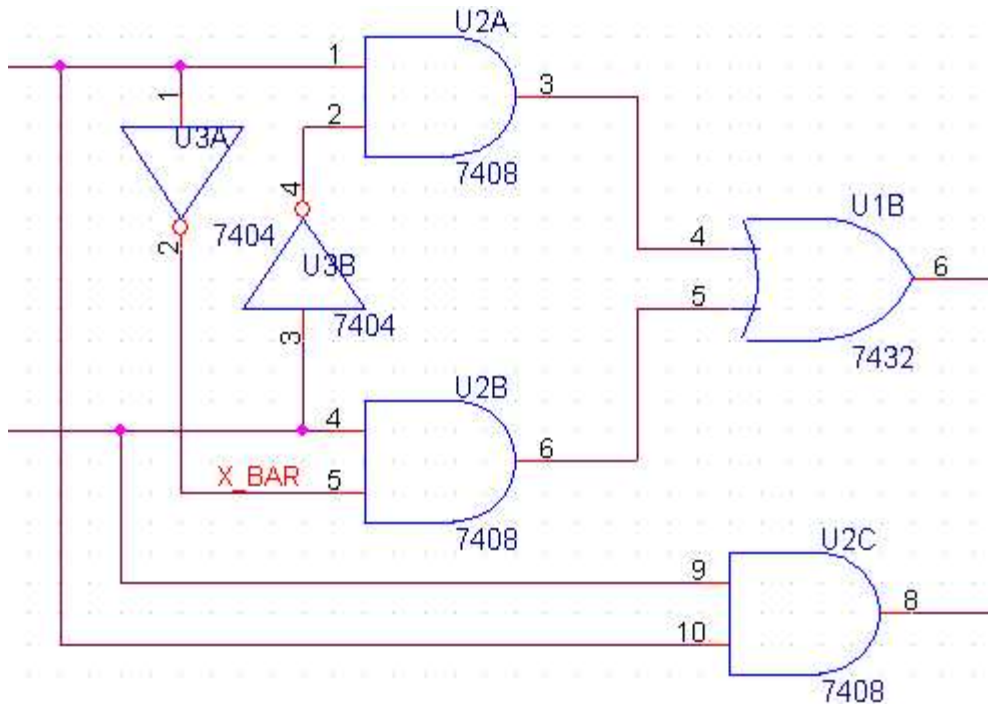
To stop wiring, right-click and select *End Wire*. The pointer changes to the default arrow.

Adding ports

To add input and output ports to the design, complete the following sequence of steps:

From the *Place* menu in Capture, select *Hierarchical Port*.

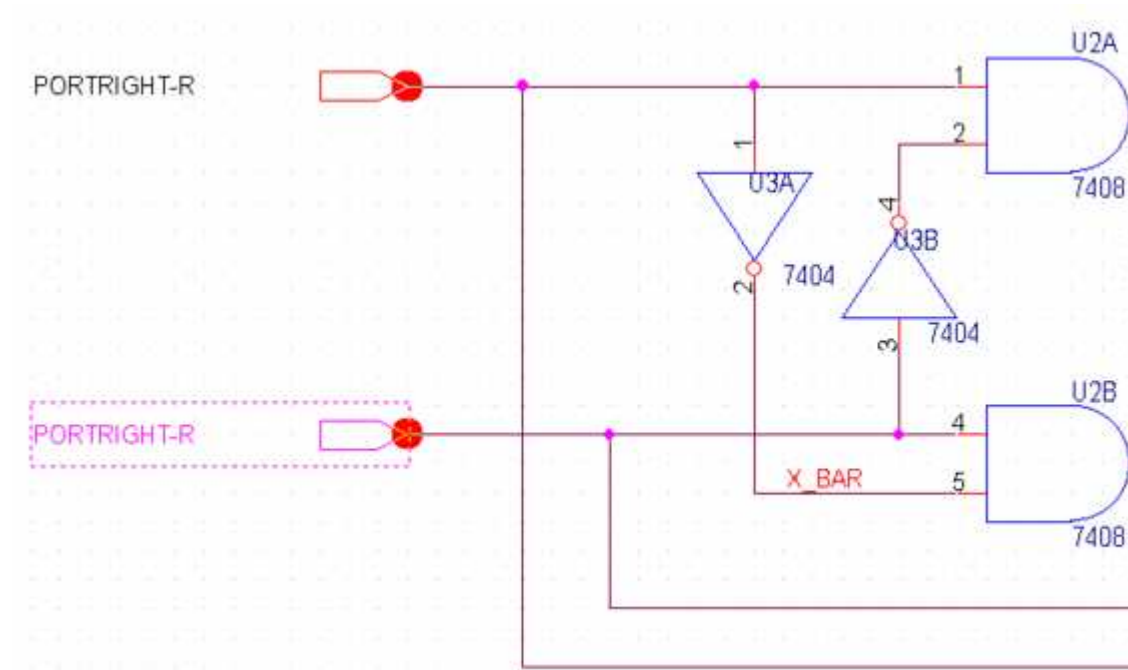The Place Hierarchical Port dialog box appears.

Note: Alternatively, you can select the Place port button from the Tool Palette.

From the Libraries list box, select CAPSYM.

First add input ports. From the Symbols list, select `PORTRIGHT-R` and click OK.

Place two instances of the port as shown in the figure below

Right-click and select *End Mode*.

To rename the ports to indicate input signals X and Y, double-click the port name.

In the Display Properties dialog box, change the value of the Name property to X and click OK.

Note: You can also use the Property Editor to edit the property values of a component. To know the details, see *OrCAD Capture User's Guide*.

Similarly, change the name of the second port to Y.

Note: You cannot use the Place Part dialog box for placing ports, because ports in CAPSYM.OLB are only symbols and not parts. Only parts are listed in the Place Part dialog box.

Add two output ports as shown in the figure below. To do this, select `PORTLEFT-L` from the CAPSYM library.

Rename the ports to SUM and CARRY, respectively.

Save the design.

The half adder design is ready. The next step is to create a full adder design that will use the half adder design.

Creating a hierarchical design

In Capture, you can create hierarchical designs using one of the following methods:

[Bottom-up method](#)

[Top-down method](#)

Another method of creating a hierarchical design is to create parts or symbols for the designs at the lowest level, and save the symbols in a user-defined library. You can later add the user-defined library in your projects and use these symbols in the schematic. For example, you can create a part for the half adder design and then instead of hierarchical blocks, use this part in the schematic. To know more about this approach, see [Generating parts for a schematic](#).

In this section, we will create the full adder hierarchical design. The half adder design created in the [Creating a flat design](#) section will be used as the lowest level design.

Bottom-up method

When you create a hierarchical design using the bottom-up methodology, you need to follow these steps.

Create the lowest-level design.

Create higher-level designs that instantiate the lower-level designs in the form of hierarchical blocks.

In this section, we will create a full adder design using bottom-up methodology. The steps involved are:

Creating a project in Capture. To view the steps, see [Creating a project](#).

Creating the lowest-level design. In the full adder design example, the lowest-level design is the half adder design. To go through the steps for creating the half adder design, see [Creating a flat design](#).

Creating the higher-level design. Create a schematic for the full adder design that uses the half adder design created in the previous step. To go through the steps, see [Creating the full adder design](#).

Creating the full adder design

In the Project Manager window, right-click on `fulladd.dsn` and select *New Schematic*.

In the New Schematic dialog box, specify the name of the new schematic folder as `FULLADD` and click OK.

In the Project Manager window, the FULLADD folder appears below `fulladd.dsn`.

Save the design.

To make the full adder circuit as the root design (high-level design), right-click on FULLADD and from the pop-up menu select *Make Root*.

The FULLADD folder moves up and a forward slash appears in the folder.

Right-click on FULLADD and select *New Page*.

In the New Page in schematic: FULLADD dialog box, specify the page name as *FULLADD* and click OK.

A new page, FULLADD, gets added below the schematic folder FULLADD.

Double-click the FULLADD page to open it for editing.

From the *Place* menu, choose *Hierarchical Block*.

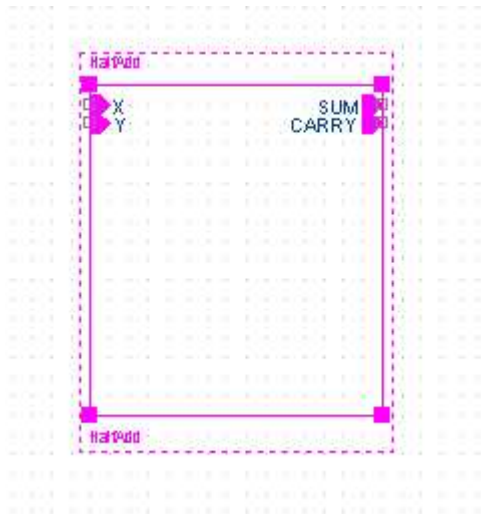In the Place Hierarchical Block dialog box, specify the reference as `HALFADD_A1`.

Specify the Implementation Type as Schematic View.

Specify the Implementation name as `HALFADD` and click OK.

The cursor changes to a crosshair.

Draw a rectangle on the schematic page.

A hierarchical block with input and output ports is drawn on the page.

If required, resize the block. Also, reposition the input and output ports on the block.

Note: To verify if the hierarchical block is correct, right-click on the block and select *Descend Hierarchy*. The half adder design you created earlier should appear.

Place another instance of the hierarchical block on the schematic page.

  Select the hierarchical block.

  From the *Edit* menu, choose *Copy*.

  From the *Edit* menu, choose *Paste*.

  Place the instance of the block at the desired location.

 **Note:** Alternatively, you can use the `<CTRL>+<C>` and `<CTRL>+<V>` keys to copy-paste the block.

By default, the reference designator for the second hierarchical block is HALFADD_A2. Double-click on the reference designator, and change the reference value to `HALFADD_B1`.

Using the Place Part dialog box, add an OR gate (7432) to the schematic. (See Figure 2-2.)

To connect the blocks, add wires to the circuit. From the *Place* menu, choose *Wire*.

Draw wires from all four ports on each of the hierarchical blocks.

Add wires until all the connections are made as shown in the figure below.
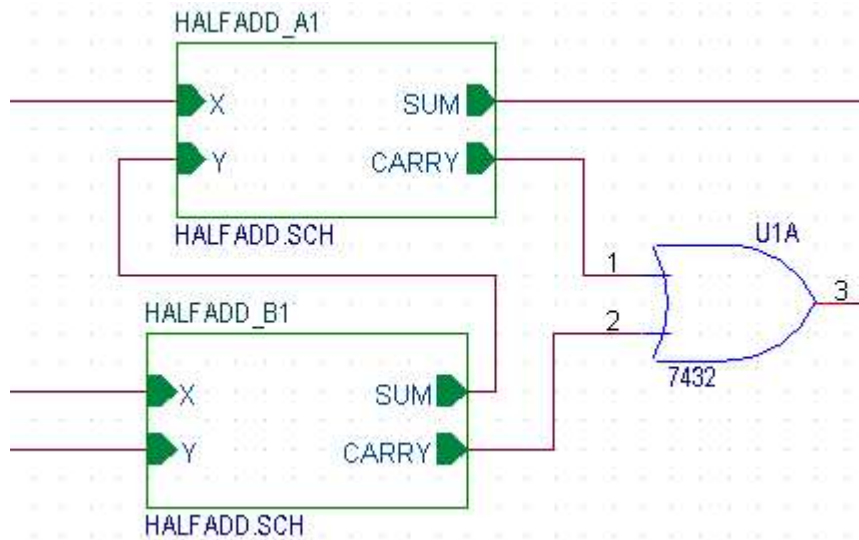
Add stimulus to the design. In the Place Part dialog box, use the Add Library button to add SOURCSTM.OLB to the design.

This library is located at *<install_dir>/tools/capture/library/pspice*.

From the Part List, select `DigStim1` and click OK.

The symbol gets attached to the cursor.

Place the symbol at three input ports: port X of the HALFADD_A1, port X and Y of HALFADD_B1.

Right-click on the schematic and select *End Mode*.

Specify the value of the Implementation property as Carry, X, and Y, respectively. See Figure 2-2.

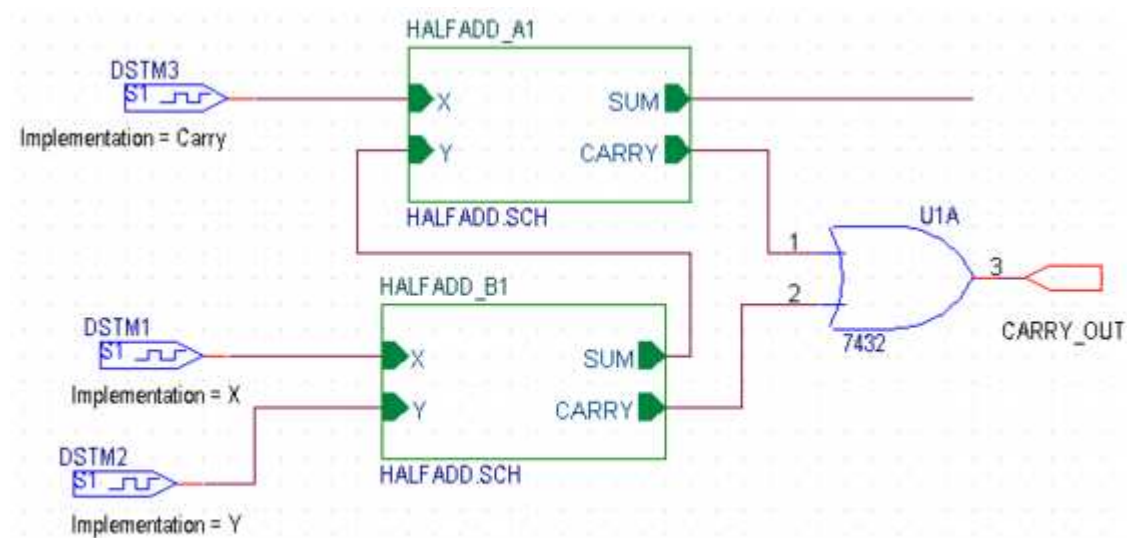Select the Place Port button, to add an output port, CARRY_OUT, to the output of the OR gate. (See Figure 2-2.)

From the list of libraries, select CAPSYM.

From the list of symbols, select PORTLEFT-L and click OK.

Place the output port as shown in the Figure 2-2.

Double-click the port name and change the port to CARRY_OUT.

Save the design.

Figure 2-2 The full adder circuit

We have only added digital components to the design so far. We will now add a bipolar junction transistor to the SUM port of the HALFADD_A1 block.

Select the Place Part tool button.

In the Place Part dialog box, select the Add Library button.

Select `ANALOG.OLB` and `BIPOLAR.OLB` and click Open.

From the part list, add resistor R. Place this resistor on the schematic and connected one end of the resistor to the SUM port of HALFADD_A1. See Figure 2-3.

From the `BIPOLAR.OLB`, select `Q2N2222` and place it on the schematic. See Figure 2-3.

Complete the circuit by adding a collector resistance, Collector Voltage, and ground. See Figure 2-3.

Adding Collector Voltage

To add the voltage, add the `SOURCE.OLB` library to the project.

From the Part List select VDC and click OK.

Place the voltage source on the schematic. See Figure 2-3.

By default, the source is of 0 volts. Using the Property Editor, change it to a voltage source of 5V. To do this, double-click the voltage source.

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In the Property Editor window, change the value of the DC parameter to 5.

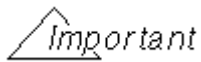Save and close the Property Editor window.

Adding Ground

To add ground, select the Place ground [GND] button.

In the Place Ground dialog box, select the `SOURCE` library.

From the part list, select `0` and click OK.

Place the ground symbol on the schematic. See Figure 2-3.

⚠ *Important* You must use the `0` ground part from the `SOURCE.OLB` part library. You can use any other ground part only if you change its name to 0.

Add a connector CON2 to the circuit. To do this, add a Capture library, `CONNECTOR.OLB` to the project.

`CONNECTOR.OLB` is located at *<install_dir>/tools/capture/library*.
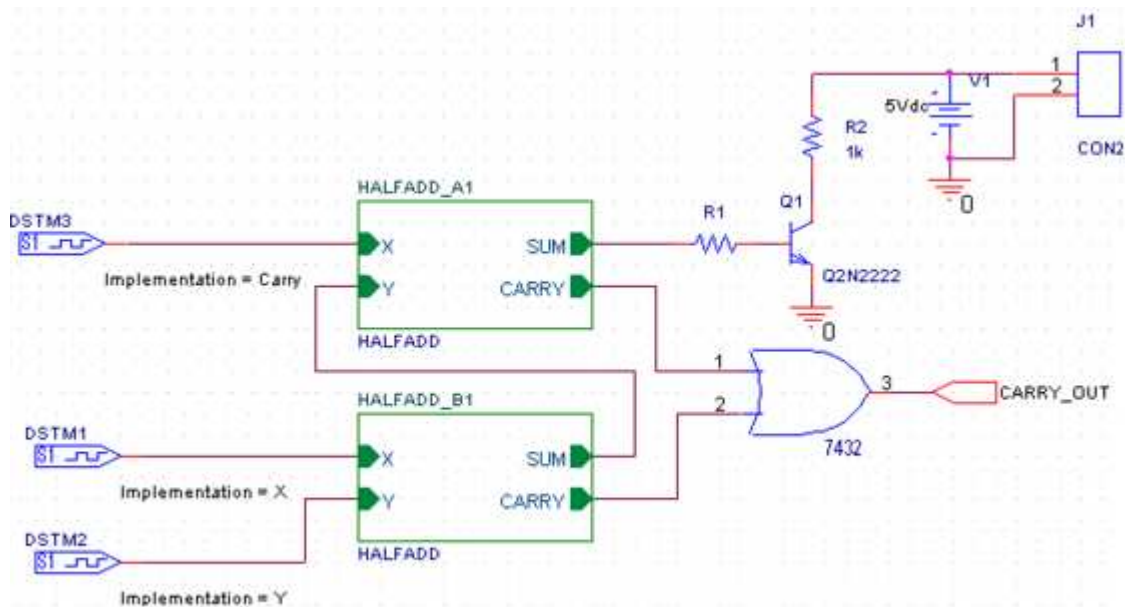
Figure 2-3 Full adder circuit with output through a transistor

You have successfully created the full adder hierarchical design using the bottom-up methodology. As the components used in this design are from the PSpice library, you can simulate this design using PSpice.

Top-down method

When you create a hierarchical design using the top-down methodology, use the following

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sequence of steps:

Create the top-level design using functional blocks, the inputs and outputs of which are known.

Create a schematic design for the functional block used in the top-level design.

This section provides an overview of the steps to be followed for creating a full adder using top-down methodology.

Create a FullAdd project.
To view the steps, see Creating a project.

Create the top-level design, using the following steps:

From the *Place* menu, choose *Hierarchical Block*.

Note: Alternatively, you can select the Place hierarchical block button from the Tool Palette.

In the Place Hierarchical Block dialog box, specify the reference as HALFADD_A1, Implementation Type as Schematic View, Implementation name as HALFADD, and click OK.

See step 9 to step 11 in the Bottom-up method section.

Draw the hierarchical block as required.

Note that unlike the hierarchical block drawn in the bottom-up methodology, the hierarchical block in the top-down methodology does not have port information attached to it.

Select the hierarchical block and then from the *Place* menu, choose *Hierarchical Pins*.

In the Place Hierarchical Pin dialog box, specify the pin name as X, Type as Input, and Width as Scalar and click OK.

Place the pin as shown in the figure below.
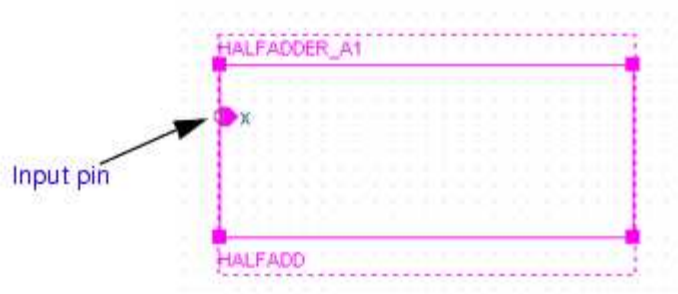
Similarly, add another input pin Y and two output pins, SUM and CARRY, as shown in the figure below.
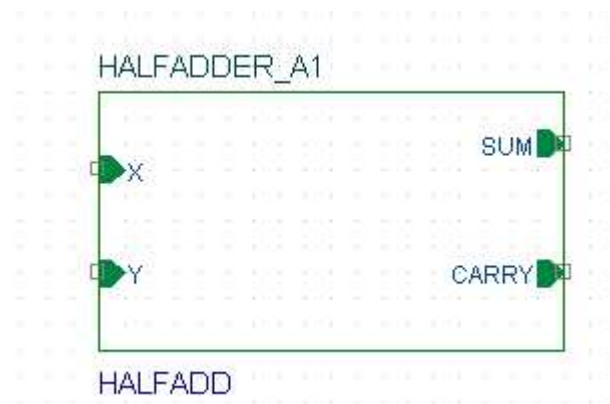
Place another hierarchical block with the Implementation Type as HALFADD. The easiest way to do this is to copy the existing hierarchical block and paste it on the schematic page.

By default, the reference value of the second hierarchical block is HALFADD_A2. Change this value to HALFADD_B1.
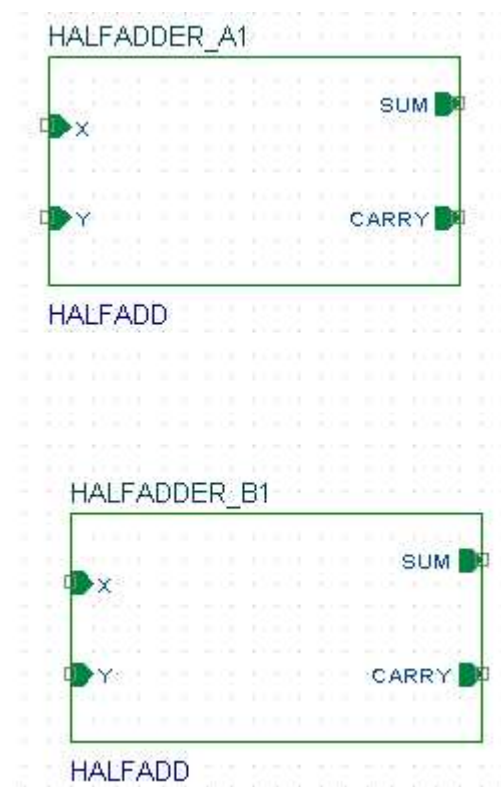
Complete the full adder circuit by adding ports, wires, and stimuli. See The full adder circuit.

Save the design.

Draw the lowest-level design using the steps listed below. For the full adder design example, the lowest-level design is a half adder circuit.

To draw the half adder design, right-click on any one of the HALFADD hierarchical block.

From the pop-up menu, select *Descend Hierarchy*.

The New Page in Schematic: 'HALFADD' dialog box appears.

Specify the page name as HALFADD and click OK.

A new schematic pages appears with two input ports, X and Y, and two output ports, SUM and CARRY.
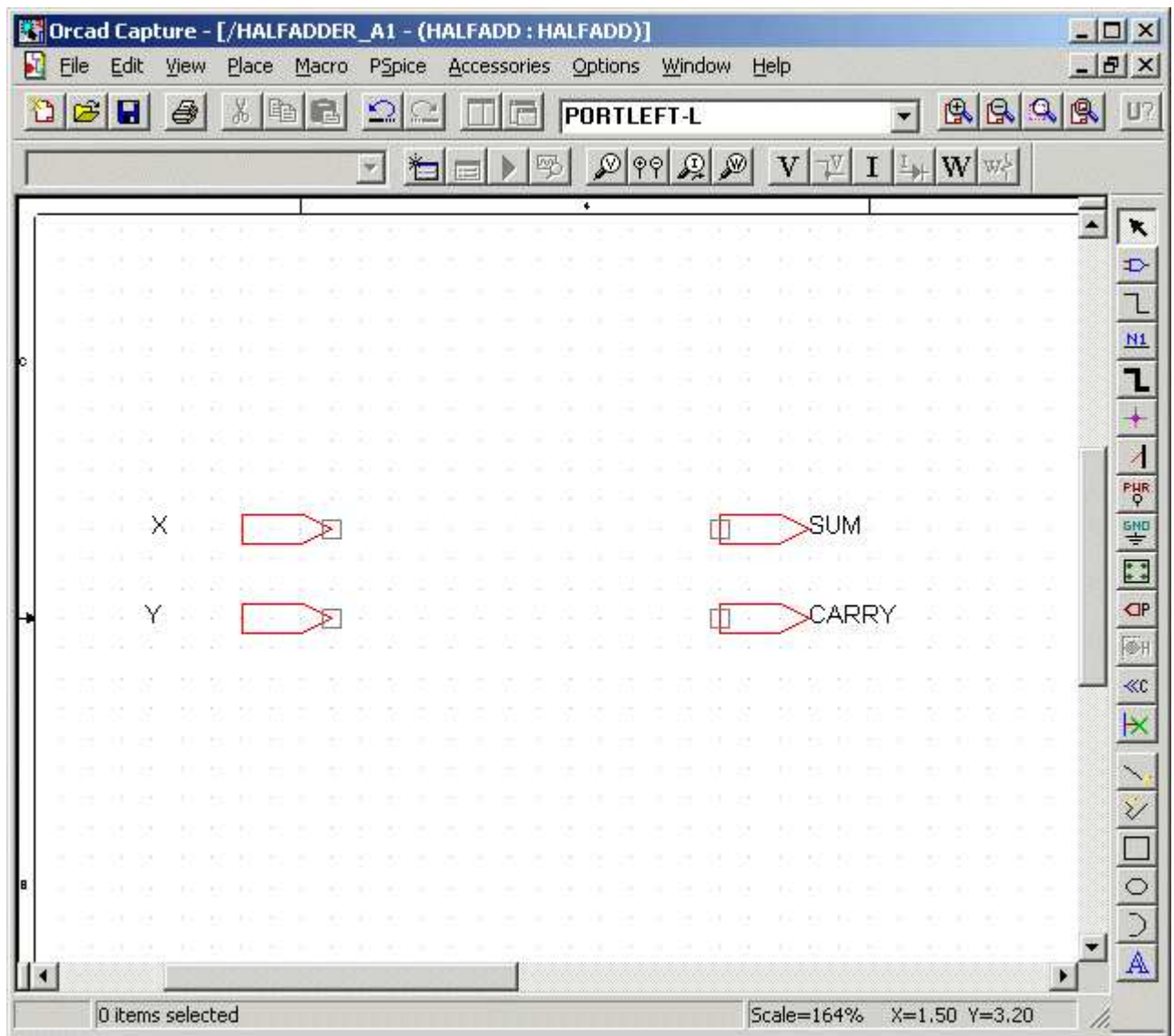
You can now draw the half adder circuit on this schematic page using the steps covered in the Creating a flat design. Also see Figure 2-1.

In the Project Manager window, a new schematic folder HALFADD gets added below `fulladd.dsn`.
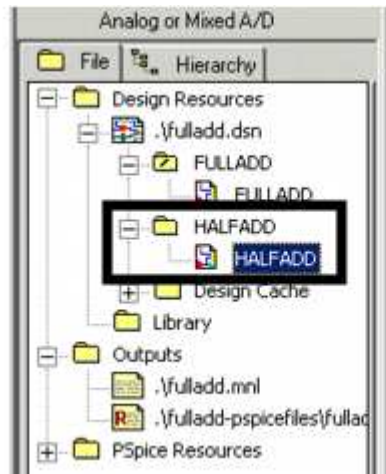
Generating parts for a schematic

Instead of creating a hierarchical block for the half adder design, you can generate a part for the half adder design and then reuse the part in any design as and when required.

In this section of the tutorial, we will generate a part for the half adder circuit that you created in the Creating a flat design section of this chapter.

To generate a part from a circuit, complete the following steps.

In the Project Manager window, select the HALFADD folder.

From the *Tools* menu, choose *Generate Part*.

In the Generate Part dialog box, specify the location of the design file that contains the circuit for which the part is to be made.

For this design example, specify the location of `fulladd.dsn`.

In the *Netlist/source file type* drop-down list box, specify the source type as `Capture Schematic Design`.
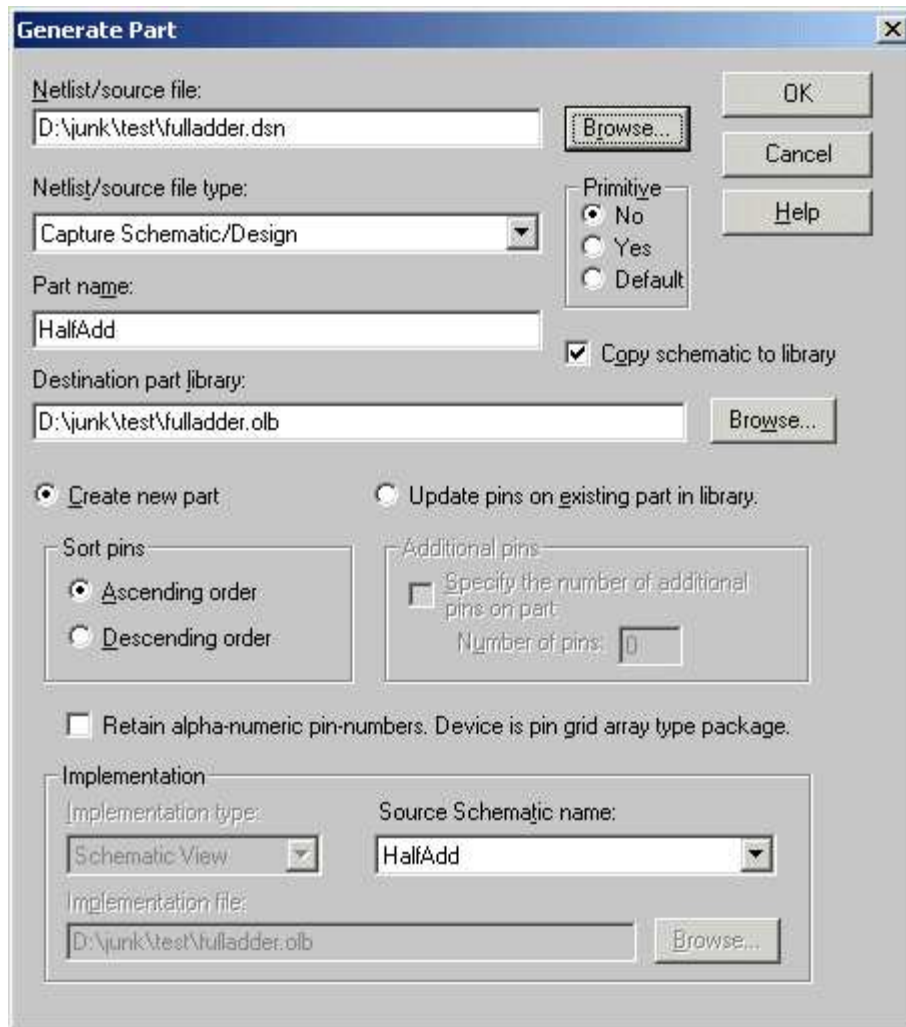
In the *Part Name* text box, specify the name of the part that is to be created, as `HALFADD`.

Specify the name and the location of the library that will contain this new part being created. For the current design example, specify the library name as `fulladd.olb`.

If you want the source schematic to be saved along with the new part, select the *Copy schematic to library* check box. For this design, select the check box.

Ensure that the *Create new part* option is selected.

To specify the schematic folder that contains the design for which the part is to be made, select HALFADD from the Source Schematic name drop-down list box.

Click OK to generate the HalfAdd part.

A new library, `fulladd.olb`, is generated and is visible under the Outputs folder in the Project Manager window. The new library also gets added in the Place part dialog box. You can now use the Place part dialog box to add the half adder part in any design.

Navigating through a hierarchical design

To navigate to the lower levels of the hierarchy, right-click a hierarchical block and choose *Descend Hierarchy*.

Similarly, to move up the hierarchy, right-click and select *Ascend Hierarchy*.

The *Ascend Hierarchy* and *Descend Hierarchy* menu options are also available in the *View* drop-down menu.

While working with hierarchical designs, you can make changes to the hierarchical blocks as well as to the designs at the lowest level.

To keep the various hierarchical levels updated with the changes, you can use the Synchronize options available in the View drop-down menu.

Select *Synchronize Up* when you have made changes in the lowest-level design and want these changes to be reflected higher up in the hierarchy.

Select *Synchronize Across* when you have made changes in a hierarchical block and want the changes to be reflected across all instances of the block.

Select *Synchronize Down* when you have made changes in a hierarchical block and want these changes to be reflected in the lowest-level design.

Processing a design

After you have created your schematic design, you may need to process your design by adding information for tasks such as, simulation, synthesis, and board layout. This section covers some of the tasks that you can perform in OrCAD Capture while processing your design.

Adding part references

To be able to take your schematic design to Layout or PCB Editor for packaging, you need to ensure that all the components in the design are uniquely identified with part references. In OrCAD Capture you can assign references either manually or by using the Annotate command.

In the full adder design, annotation is not required at this stage because by default, unique part references are attached to all the components. This is so because by default, Capture adds part reference to all the components placed on the schematic page. If required, you can disable this feature by following the steps listed below.

From the *Options* menu, choose *Preferences*.

In the Preferences dialog box, select the Miscellaneous tab.

In the Auto Reference section, clear the *Automatically reference placed parts* check box.

Click OK to save these settings.

In case the components in your design do not have unique part references attached to them, you must run the Annotate command.

To assign unique part references to the components in the FULLADD design using the Annotate command, complete the following steps:

In the Project Manager window, select the `fulladd.dsn` file.

From the *Tools* drop-down menu, choose *Annotate*.

Note: Alternatively, you can click the Annotate button on the toolbar.

In the Packaging tab of the Annotate dialog box, specify whether you want the complete design or only a part of the design to be updated. Select the *Update entire design* option button.

In the Actions section, select the *Incremental reference update* option button.

Note: To know about other available options, see the dialog box help.

The full adder design is a complex hierarchical design. So choose the *Update Occurrence* option button.

Note: When you select the Update Occurrence option, you may receive a warning message. Ignore this message because for all complex hierarchical designs, the occurrence mode is the preferred mode.

For the rest of the options, accept default values and click OK to save your settings.

The Undo Warning message box appears.

Click Yes.

A message box stating that the annotation will be done appears.

Click OK.

Your design is annotated and saved. You can view the value of updated cross reference designators on the schematic page.

Caution — *If you select the Annotate command after generating the Layout or PCB Editor netlist, you will receive an error message stating that annotating at this stage may cause the board to go out of sync with the schematic design. This may cause further backannotation problems.*

Creating a cross reference report

Using Capture, you can create cross reference reports for all the parts in your design. A cross reference report contains information, such as part name, part reference, and the library from which the part was selected.

To generate a cross reference report using Capture:

From the Tools menu choose Cross References.

Alternatively, you can choose the cross reference parts button from the toolbar.

In the Cross Reference Parts dialog box, ensure that the *Cross reference entire design* option button is selected.

Note: If you want to generate the cross reference report for a particular schematic folder, select the schematic folder before opening the Cross Reference Parts dialog box, and then select the cross reference selection option button.

In the Mode section, select the *Use Occurrences* option button.

Note: Ignore the warning that is displayed when you select the Use Occurrences mode. For complex hierarchical designs, you must always use the occurrence mode.

Specify the report that you want to be generated.

In case you want the report to be displayed automatically, select the View Output check box.

Click OK to generate the report.
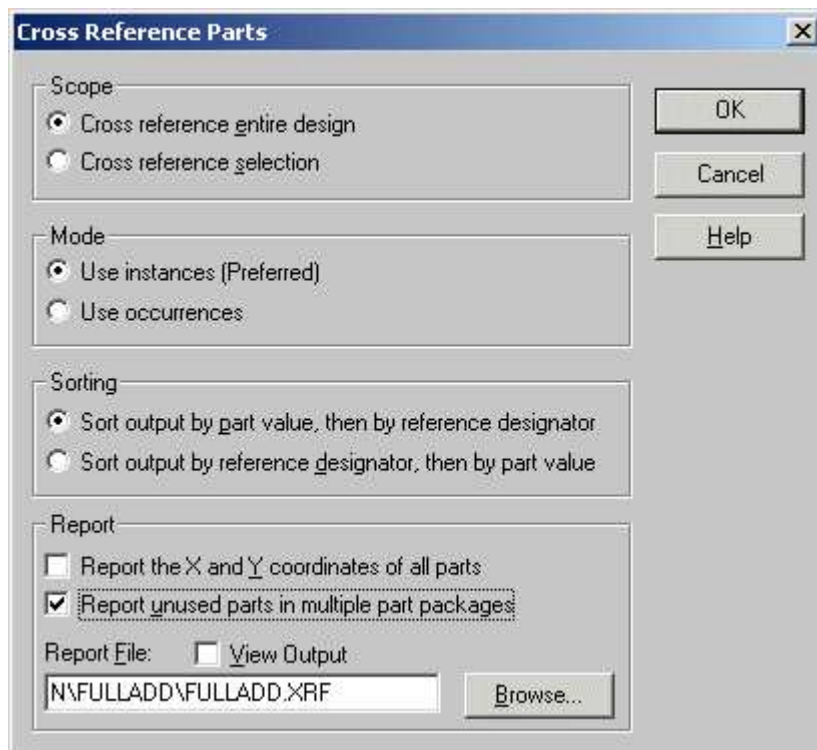
A sample output report is shown below.

```
FULLADD.XRF - Notepad
File  Edit  Format  Help

  Revised: Wednesday, January 28, 2004
        Revision:

Design Name:  D:\FULLADDDESIGN\FULLADD.DSN

Cross Reference       January 28,2004      12:02:24      Page1

Item      Part      Reference          SchematicName   Sheet    Library
_____

1         1K        R1        /FULLADD          1        C:\ORCAD\ORCAD_10.0_DEMO\TOOLS\CAPTURE\LIBRARY
2         1K        R2        /FULLADD          1        C:\ORCAD\ORCAD_10.0_DEMO\TOOLS\CAPTURE\LIBRARY
3         7404      U3A       HALFADD_A1/HALFADD   2         C:\ORCAD\ORCAD_10.0_DEMO\TOOLS\CAPTURE
4         7404      U3B       HALFADD_A1/HALFADD   2         C:\ORCAD\ORCAD_10.0_DEMO\TOOLS\CAPTURE
5         7404      U3C       HALFADD_B1/HALFADD   3         C:\ORCAD\ORCAD_10.0_DEMO\TOOLS\CAPTURE
6         7404      U3D       HALFADD_B1/HALFADD   3         C:\ORCAD\ORCAD_10.0_DEMO\TOOLS\CAPTURE
7         7408      U2A       HALFADD_A1/HALFADD   2         C:\ORCAD\ORCAD_10.0_DEMO\TOOLS\CAPTURE
8         7408      U2B       HALFADD_A1/HALFADD   2         C:\ORCAD\ORCAD_10.0_DEMO\TOOLS\CAPTURE
9         7408      U2C       HALFADD_A1/HALFADD   2         C:\ORCAD\ORCAD_10.0_DEMO\TOOLS\CAPTURE
10        7408      U2D       HALFADD_B1/HALFADD   3         C:\ORCAD\ORCAD_10.0_DEMO\TOOLS\CAPTURE
11        7408      U4A       HALFADD_B1/HALFADD   3         C:\ORCAD\ORCAD_10.0_DEMO\TOOLS\CAPTURE
12        7408      U4B       HALFADD_B1/HALFADD   3         C:\ORCAD\ORCAD_10.0_DEMO\TOOLS\CAPTURE
13        7432      U1A       /FULLADD          1        C:\ORCAD\ORCAD_10.0_DEMO\TOOLS\CAPTURE\LIBRARY
```

Generating a bill of materials

After you have finalized your design, you can use Capture to generate a bill of materials (BOM). A bill of materials is a composite list of all the elements you need for your PCB design. Using Capture, you can generate a BOM report for electrical and as well as non-electrical parts, such as screws. A standard BOM report includes the item, quantity, part reference, and part value.

To generate a BOM report:

In the Project Manager window, select `fulladd.dsn`.

From the *Tools* menu, select *Bill of Materials*.

To generate a BOM report for the complete design, ensure that the Process entire design option button is selected.

For a complex hierarchical designs, the preferred mode is the occurrence mode. Therefore, select the *Use Occurrences* option button.
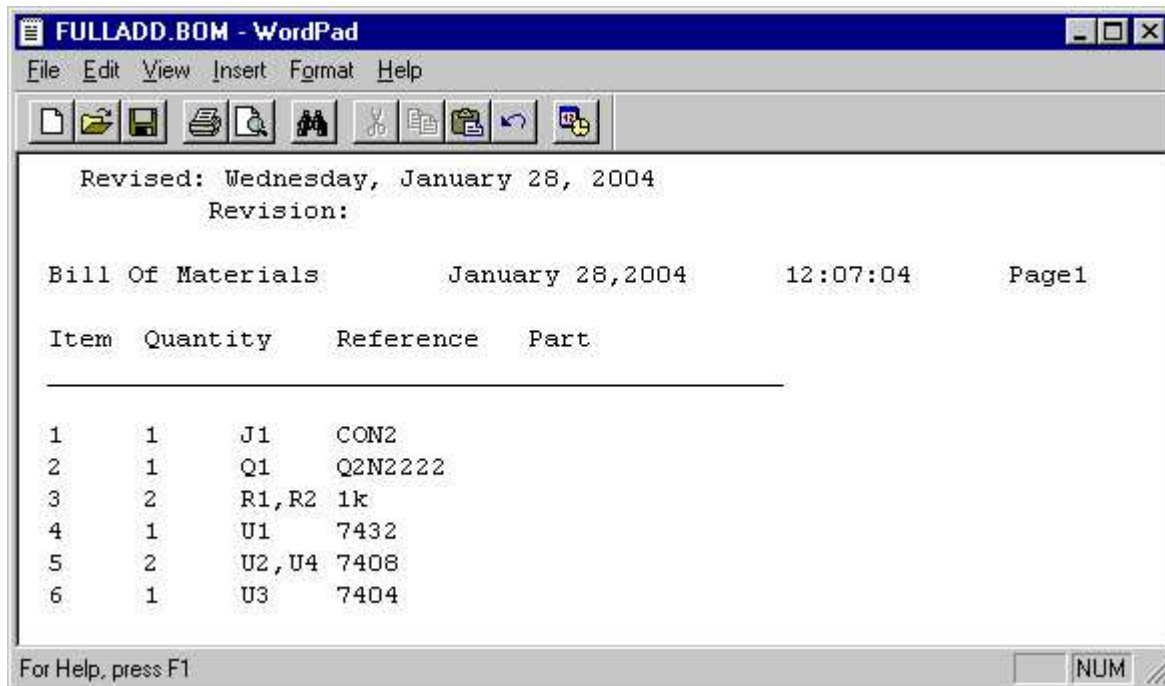
Note: In case you receive a warning stating that it is not the preferred mode, ignore the warning.

Specify the name of the BOM report to be generated. For the current design, accept the default name, `FULLADD.BOM`.

Note: By default, the report is named as *designname.BOM*.

Click OK.

The BOM report is generated. A sample report is shown below:

```
FULLADD.BOM - WordPad
File  Edit  View  Insert  Format  Help

   Revised: Wednesday, January 28, 2004
            Revision:

Bill Of Materials          January 28,2004      12:07:04      Page1

Item   Quantity       Reference    Part
   _____

1       1       J1      CON2
2       1       Q1      Q2N2222
3       2       R1,R2   1k
4       1       U1      7432
5       2       U2,U4   7408
6       1       U3      7404

For Help, press F1                                          NUM
```

Getting your design ready for simulation

To be able to simulate your design using PSpice, you must have the connectivity information and the simulation settings for the analysis type to be done on the circuit design.

The simulation setting information is provided by a simulation profile (*.SIM). This section covers the steps to be followed in Capture for creating a simulation profile.

Note: To know more details about getting your design ready for simulation using PSpice, see *Chapter 3, Preparing a design for simulation* of the *PSpice User's Guide*.

Creating a simulation profile from scratch

To create a new simulation profile to be used for transient analysis, complete the following steps:

From the PSpice menu in Capture, choose New Simulation Profile.

In the New Simulation dialog box, specify the name of the new simulation profile as TRAN.

In the Inherit From text box, ensure that none is selected and click Create.

The Simulation Setting dialog box appears with the Analysis tab selected.

In the Analysis type drop-down list box, Time Domain (Transient) is selected by default. Accept the default setting.

Specify the options required for running a transient analysis. In the Run to time text box, specify the time as 100u.

Click OK to save your modifications and to close the dialog box.

You can now run transient analysis on the circuit. Note that the Simulation Setting dialog box also provides you with the options for running advanced analysis, such as Monte Carlo (Worst Case) analysis, Parametric analysis and Temperature analysis. You may choose to run these as and when required.

Note: To know details about each option in the Simulation Settings dialog box, click the Help button in the dialog box.

Creating a simulation profile from an existing profile

You can create a new simulation profile from an existing simulation profile. This section covers the steps for creating a new simulation profile, SWEEP, from an existing simulation profile, named TRAN.

From the *PSpice* menu, choose *New Simulation Profile*.

In the New Simulation dialog box, specify the profile name as SWEEP.

In the Inherit From drop-down list box, select FULLADD-TRAN.

Click the Create button.

The Simulation Settings dialog box appears with the general settings inherited from the existing simulation profile. You can now modify the settings as required and run PSpice to simulate your circuit.

Adding Layout-specific properties

To be able to take your design to OrCAD Layout or OrCAD PCB Editor for placement and routing, you need to add the footprint information for each of the components in your design.

By default, some footprint information is available with all the components from the PSpice-compatible libraries located at *<install_dir>/tools/capture/library/pspice*. However, these footprints are not valid. You need to change these values to valid footprint values. You can add footprint information either at the schematic design stage in OrCAD Capture or during the board design stage in OrCAD Layout. In this section, you will learn to add footprint information to the design components during the schematic design stage.

To add footprint information to the OR gate, 7432, in the FULLADD schematic page, complete the following steps.

Right-click on the OR gate and select *Edit Properties*.

The Property Editor window appears.

In the Filter by drop-down list box, select Orcad-Layout.

Note: For adding PCB Editor footprints, select the Cadence-Allegro filter.

The columns in the spreadsheet display the Layout properties.

To change the value of the PCB Footprint property, click on the corresponding cell and type in the value as `SOG.050/14/WG.244/L.350`.

Press ENTER or click Apply.

Note: To assign PCB footprints to your schematic parts, select the Layout footprint names from OrCAD Layout Footprint Libraries or from your custom footprint libraries.

Save the changes and close the Property Editor window.

Similarly, add PCB footprint information for all the components in the design. The component name and the corresponding footprint information to be added is listed in the table below.

For Layout:

Component...	PCB Footprint...
AND gate (7408)	`SOG.050/14/WG.244/L.350`
OR gate (7432)	`SOG.050/14/WG.244/L.350`
NOT gate(7404)	`SOG.050/14/WG.244/L.350`
Resistance	`SM/R_0805`
Connector(CON2)	`SIP/TML/L.200/2`

For PCB Editor:

Component...	PCB Footprint...
AND gate (7408)	`SOIC14`
OR gate (7432)	`SOIC14`
NOT gate(7404)	`SOIC14`
Resistance	`RES500`

Connector(CON2)	JUMPER2
Transistor(Q2N2222)	TO18

Your design is now ready to be taken to OrCAD Layout or OrCAD PCB Editor for placement and routing.

Design rules check

After you have completed your design, it is recommended that you run design rules check (DRC) to isolate any unwanted design errors that might be there in the design.

To run DRC on the full adder design, complete the following steps:

In the Project Manager window, select the design file, `fulladd.dsn`.

From the *Tools* menu, select *Design Rule Checks*.

Note: Alternatively, you can select the Design Rule Checks button from the toolbar.

In the Design Rules Check dialog box, the Design Rules Check tab is selected by default. Specify your preferences.

By default, the *Check entire design* option button is selected. To run DRC on the complete design, accept the default selection.

Select the *Use Occurrences* option button.

Note: For complex hierarchical designs, the occurrence mode is the preferred mode. Therefore, ignore the warning that is displayed when you select the Use occurrences option button.

To run the DRC, select the *Check design rule* option button.

In the Report section, select appropriate check boxes to specify what all is required in the DRC report.

For the current design example, select the *Check unconnected nets* and *Report identical part references* check boxes.

Select the *View Output* check box.

When this check box is selected, the DRC report is opened automatically for viewing after

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the checks are complete.

In the Report File text box, specify the name and the location of the DRC file to be created.

For the current design example, specify the filename as `fulladd.dsn`.

Click OK.

After the checks are done, the DRC report is displayed in the format shown below.

```
Checking Pins and Pin Connections

--------------------------------------------------

Checking Schematic:   FULLADD

--------------------------------------------------

Checking Electrical Rules

Checking for Unconnected Nets

Checking for Invalid References

Checking for Duplicate References

Check Bus width mismatch

--------------------------------------------------

Checking Schematic: HALFADD_A1 HALFADD

--------------------------------------------------

Checking Electrical Rules

Checking for Unconnected Nets

Checking for Invalid References

Checking for Duplicate References

Check Bus width mismatch

--------------------------------------------------

Checking Schematic: HALFADD_B1 HALFADD

--------------------------------------------------

Checking Electrical Rules

Checking for Unconnected Nets

Checking for Invalid References
```

```
Checking for Duplicate References

Check Bus width mismatch
```

Summary

This chapter covered the steps for creating both flat and hierarchical designs using OrCAD Capture. In the process, you were introduced to basic design creation tasks, such as creating projects, adding libraries to a project, placing parts, and editing property values.

What's next

In the next chapter, *Simulating a design*, you will use PSpice for simulating the schematic design created in this chapter. You will be introduced to various types of simulations and their need in the PCB design cycle.

Recommended reading

For more information about OrCAD Capture, see *OrCAD Capture User's Guide* and Capture online help. To know more about OrCAD Unison flow, see the *OrCAD Unison Suites Flow Guide*. Return to top of page

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